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09/718,008	11/21/2000	Kenneth Perlin	KPER-4	9323

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EXAMINER	
WANG, JIN CHENG	
ART UNIT	**PAPER NUMBER**
2672	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/718,008	PERLIN, KENNETH	
	Examiner	Art Unit	
	Jin-Cheng Wang	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's submission filed on 10/20/2004 has been entered. Claims 1-12 are pending in the application.

Response to Arguments

Applicant's arguments filed October 20, 2004 have been fully considered but are not found persuasive in view of the ground(s) of rejection set forth in the last Office Action.

For example, the term "each 3 dimensional evaluation requires only one clock cycle" in Claim 1 is a relative term which renders the claim *indefinite.* The term "each 3 dimensional evaluation requires only one clock cycle" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Since "each 3 dimensional evaluation requires only one clock cycle" is not defined in the specification and the claim, the speed for each evaluation in a computer software or hardware cannot be ascertained if the computer **software or hardware** being used in performing the evaluation is not determined or if "each 3 dimensional evaluation" is not clearly defined in the claim.

Moreover, performing "each 3 dimensional evaluation" in the steps presented in the Claim 1 is not clearly construed because it cannot be determined what applicant is meant by "each 3 dimensional evaluation". It could refer to each of the steps recited in the Claim 1. It is not clear whether "each 3 dimensional evaluation" refer to the **entire** computation time for obtaining a "new Perlin Noise" result or the computation time for performing an individual step of the numerous steps involved in calculating a "new Perlin Noise" result.

Applicant argues that it is stated in the specification, "one clock cycle is generally 200-300 MHz." Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant further argues that, "it further states that the device computes a Perlin noise value, with a throughput of one result per clock cycle." However, the claim limitations set forth in the claim 1 recite "each 3 dimensional evaluation" which reads differently from computing a Perlin noise value as stated in the specification.

Since the claim limitation of "each 3 dimensional evaluation requires only one clock cycle" is indefinite, it carries no patentable weight. The computation time is relative to the computer **software or hardware** used for performing each 3 dimensional evaluation. Moreover, it cannot be ascertained what applicant is meant by "each 3 dimensional evaluation" as recited in the claim 1. There is no clear definition of each 3 dimensional evaluation." However, Ye teaches in page 113 the 3-D rendering system implemented on the TM-2 which is comprising Altera 10K50 FPGAs and four banks of 65-bit wide SRAM and the resources used in the implementation include on workstation, all four FPGAs on the TM-2, one bank of TM-2 SRAM, a VGA card and a monitor. Ye discloses in page 118 that the procedure texture generator can produce one pixel of texture for **every four clock cycles.**

Claim Rejections - 35 USC § 112 (First Paragraph)

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description and enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. For example, the claim limitation that "each 3 dimensional evaluation requires only one clock cycle" lacks adequate disclosure in the specification.

The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim limitation that "each 3 dimensional evaluation requires only one clock cycle" is not enabled by the specification.

For example, on page 7 of the specification, Applicant describes that Intel Corporation has implemented the Perlin Noise over the 2-dimensional that requires 32 clock cycles per 2D evaluation, while the present invention requires only one clock cycle per 3D evaluation. However, the hardware used in the implementation of the new Perlin Noise is not clearly described. It is not clear whether applicant's "evaluation" set forth in the claim 1 is implemented in software using the Intel/MMX technology or a dedicated hardware such as a certain number FPGAs.

Moreover, performing "each 3 dimensional evaluation" in the steps presented in the Claim 1 is not clearly construed because it cannot be determined what applicant is meant by "each 3 dimensional evaluation". It could refer to each of the steps recited in the Claim 1. It is not clear whether "each 3 dimensional evaluation" refer to the entire computation time for

obtaining a new Perlin Noise result or the computation time for performing an individual step of the numerous steps involved in calculating a "new Perlin Noise" result.

Claims 2-11 depend on the Claim 1 and are rejected due to their dependency on the Claim 1. Claim 12 is subject to the same rationale of rejection set forth in the Claim 1 because it set forth the same limitation as the Claim 1.

Claim Rejections - 35 USC § 112 (Second Paragraph)

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term " each 3 dimensional evaluation requires only one clock cycle " in Claim 1 is a relative term which renders the claim *indefinite*. The term " each 3 dimensional evaluation requires only one clock cycle " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Since "each 3 dimensional evaluation requires only one clock cycle" is not defined in the specification and the claim, the speed for each evaluation in a computer software or hardware cannot be ascertained if the computer **software or hardware** being used in performing the evaluation is not determined.

Moreover, performing "each 3 dimensional evaluation" in the steps presented in the Claim 1 is not clearly construed because it cannot be determined what applicant is meant by

"each 3 dimensional evaluation". It could refer to each of the steps recited in the Claim 1. It is not clear whether "each 3 dimensional evaluation" refer to the entire computation time for obtaining a new Perlin Noise result or the computation time for performing an individual step of the numerous steps involved in calculating a "new Perlin Noise" result.

Claims 2-11 depend on the Claim 1 and are rejected due to their dependency on the Claim 1. Claim 12 is subject to the same rationale of rejection set forth in the Claim 1 because it set forth the same limitation as the Claim 1.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Andy G. Ye and David M. Lewis "Procedural Texture Mapping on FPGAs", ACM 1999, 1-58113-088-0/99/02, page 112-120 (hereinafter Ye).

7. Claim 1:

Ye teaches a method for creating an appearance of texture in a computer image (see e.g., figures 11-14) comprising the steps of:

Inputting a point {xd} in D-dimensional geometric space R^3 described via D M bit quantities id and D N bit quantities ud, where id are M bit representations of greatest integers not > xd, and ud are N bit representations of remainders (xd – id), where M and N are integers > 3 and D = 3, in a computer (page 116);

Computing a pseudo-random hash value at each vertex of a unit cube C surrounding the point (figure 8);

Computing a contribution from each vertex using the hash-value (figure 6);

Combining with the computer the contribution from each vertex into a single interpolated result (page 115-116) so that each 3 dimensional evaluation requires only one clock cycle (Since the claim limitation of "each 3 dimensional evaluation requires only one clock cycle" is indefinite, it carries no patentable weight. The computation time is relative to the computer software or hardware used for performing each 3 dimensional evaluation. Moreover, it cannot be ascertained what applicant is meant by "each 3 dimensional evaluation" as recited in the claim 1. There is no clear definition of each 3 dimensional evaluation." *However, Ye teaches in page 113 the 3-D rendering system implemented on the TM-2 which is comprising Altera 10K50 FPGAs and four banks of 65-bit wide SRAM and the resources used in the implementation include on workstation, all four FPGAs on the TM-2, one bank of TM-2 SRAM, a VGA card and a monitor. Ye discloses in page 118 that the procedure texture generator can produce one pixel of texture for* ***every four clock cycles.***)

8. Claim 12:

Ye teaches an apparatus for creating an appearance of texture in a computer image (pages 117-118) comprising:

A computer (pages 117-118);

A mechanism for inputting a point {xd} in D-dimensional geometric space R^3 (a Perlin noise function of three-dimensional space; see page 115) described via D M bit quantities id and D N bit quantities ud, where id are M bit representations of greatest integers not > xd, and ud are N bit representations of remainders (xd – id), where M and N are integers > 3 and D = 3, in a computer (See Perlin Noise Function of pages 115-116);

A mechanism for computing a pseudo-random hash value (e.g., pseudo-random function values using xor tables) at each vertex of a unit cube C (corners of a grid cell) surrounding the point (See the Random Number Generator of figure 8);

A mechanism for computing a contribution from each vertex using the hash-value (hash values being used for interpolation. See figure 6);

A mechanism for combining with the computer the contribution from each vertex into a single interpolated result (See in particular the linear interpolation unit output of figure 6 and 7; page 115-116) so that each 3 dimensional evaluation requires only one clock cycle (Since the claim limitation of "each 3 dimensional evaluation requires only one clock cycle" is indefinite, it carries no patentable weight. However, Ye teaches in page 113 the 3-D rendering system implemented on the TM-2 which is comprising Altera 10K50 FPGAs and four banks of 65-bit wide SRAM and the resources used in the implementation include on workstation, all four FPGAs on the TM-2, one bank of TM-2 SRAM, a VGA card and a monitor. Ye discloses in page

118 that the procedure texture generator can produce one pixel of texture for every *four clock cycles*).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andy G. Ye and David M. Lewis "Procedural Texture Mapping on FPGAs", ACM 1999, 1-58113-088-0/99/02, page 112-120 (hereinafter Ye).

11. Claims 2-4:

(1) Ye teaches a method of hardware texture mapping in which texture images are synthesized using FPGAs including the computing a hash value step (page 116), the computing a contribution step and the combining step.

(a) Ye teaches computing multiple n-bit pseudo-random hash values, one hash value for each of the eight vertices of the surrounding unit cube C using XOR table.

(b) Ye teaches computing for each vertex of the surrounding unit cube C the contribution of each vertex with XOR modules.

(c) Ye teaches combining the contribution from each vertex into a single result using 3 ease-curve s modules (figures 6, 9 and 10).

(2) Ye does not teach (a) six "+" modules combined with seven "L" modules; (b) three "+" modules combined with eight "H" modules; (c) the s modules.

(3) Ye however teaches (a) the "+" modules (figure 8); (b) the "L" modules and the "H" modules (figures 7 and 8); (c) the s modules (figures 6 and 10).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the various combinations of "+" modules, the "L" modules, "H" modules and the s modules into the Ye's method for hardware texture mapping because Ye suggests implementing "+" modules in figure 8, XOR modules in figure 8 and s modules in figures 6 and 10 and therefore suggesting an obvious modification.

(5) Therefore, it would have been obvious to implement Ye's method with some specific numbers/combinations of modules in different layout so that it would facilitate an efficient implementation of Perlin Noise based 3-D procedural textures.

Claim 5:

The claim 5 encompasses the same scope of invention as that of claim 4 except additional claimed limitation of a look-up table. However, Ye further discloses the claimed limitation of a look-up table (page 116).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 5 except additional claimed limitation of computing a gradient direction from each hash value. However, Ye further discloses the claimed limitation of computing a gradient direction from each hash value (page 116).

Claim 7:

The claim 7 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of allowing the inner product to be done using no multiples, only adds and shifts. However, Ye further discloses the claimed limitation of allowing the inner product to be done using no multiples, only adds and shifts (figures 6-10).

Claim 8:

The claim 8 encompasses the same scope of invention as that of claim 7 except additional claimed limitation of choosing the gradients. However, Ye further discloses the claimed limitation of choosing the gradients (page 116).

Claim 9:

The claim 9 encompasses the same scope of invention as that of claim 8 except additional claimed limitation of using 7 linear-interrelation modules L to perform a trilinear interpolation. However, Ye further discloses the claimed limitation of using 7 linear-interrelation modules L to perform a trilinear interpolation (pages 115-116).

Claim 10:

The claim 10 encompasses the same scope of invention as that of claim 9 except additional claimed limitation of computing an ease curve. However, Ye further discloses the claimed limitation of computing an ease curve (page 116).

Claim 11:

The claim 11 encompasses the same scope of invention as that of claim 10 except additional claimed limitation of linear interpolations modules. However, Ye further discloses the claimed limitation of linear interpolations modules (figure 7).

Remarks

12. Applicant's arguments, filed 04/20/2004, paper number 9, have been fully considered but they are not deemed to be persuasive.

13. Applicant argues in essence with respect to claim 1 and other related claims that:

"The Examiner has rejected Claims 1 and 12 as being anticipated by Ye and Lewis. Applicant respectfully traverses this rejection in view of the amendments to the claims. Claims 1 and 12 now have the limitation "so that each 3 dimensional evaluation requires only one clock cycle" and the geometric space is R^3. ...Ye and Lewis teach that a system based on the prior art Perlin noise function which the claimed invention improves upon is not based on a point in R^3 space...In addition, Ye and Lewis fail to teach 'so that each 3 dimensional evaluation requires only one clock cycle'."

In response to the argument, the Examiner asserts that the claim limitation of "each 2 dimensional evaluation requires only one clock cycle" set forth in the Claim 1 presents an incredible utility in the light of the knowledge of the art. The claim limitation of "each 2 dimensional evaluation requires only one clock cycle" is factually misleading. For example, the computing time for each evaluation set forth in the Claim 1 is highly dependent on software and hardware such as the CPU speed of a computer used in performing the computation wherein higher speed computer (such as a computer equipped with the Intel Pentium II) generally requires less time than lower speed computer (such as a computer equipped with 386 or 486 microprocessor) in performing each evaluation in the steps presented in the Claim 1. In addition,

it is not clear from the specification whether the evaluation is implemented in software using the Intel/MMX technology or a dedicated hardware such as a certain number of FPGAs.

The Office thus considers the asserted utility to be inconsistent with known scientific principles or speculative at best as to whether attributes of the invention necessary to impart the asserted utility were actually present in the invention. For example, each 2 dimensional evaluation is dependent on the software and hardware such as the CPU speed of the computer wherein what kind of computer being employed in performing the computation for the steps set forth in the Claim 1 is not implicitly given, therefore the computation speed can not be determined. However, the computation speed of each evaluation such as "one clock cycle" is recited in the Claim 1.

Moreover, on page 7 of the specification, Applicant describes that Intel Corporation has implemented the Perlin Noise over the 2-dimensional that requires 32 clock cycles per 2D evaluation, while the present invention requires only one clock cycle per 3D evaluation. However, the hardware used in the implementation of the new Perlin Noise is not clearly described. It is not clear whether applicant's "evaluation" set forth in the claim 1 is implemented in software using the Intel/MMX technology or a dedicated hardware such as a certain number FPGAs.

The Examiner also asserts that Ye teaches the claim limitation as set forth in the Claim 1. Ye and Lewis teaches a gate-level implementation of improved versions of Perlin Noise Function of three-dimensional space. According to Ye and Lewis, it is apparent that the original method in the prior art Perlin noise function that applicant refers to can consume quite large amounts of memory since multiple copies of the pseudo random function are needed to fully

exploit the parallelism available. Unfortunately, both the claim limitation as set forth in the present claims and applicant's argument have not identified a difference between the claim invention and the prior art Perlin noise function. The claimed invention recites an implementation similar to the texture mapping comprising the three-pipelined stages of hashing, gradient and interpolation as taught by Ye and Lewis. Therefore, the examiner asserts that Ye and Lewis meets the claim limitation as recited in claims 1 and 12. Although these claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Specifically, Applicant has not identified the claim invention to be distinguishable from the prior art of record. From the cited reference, it is concluded that Ye and Lewis fulfills the claims 1 and 12 as currently drafted.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (571) 272-7665. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jcw

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